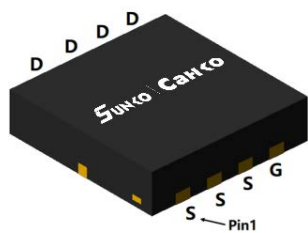
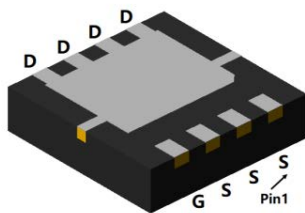


N-Channel Enhancement Mode Field Effect Transistor

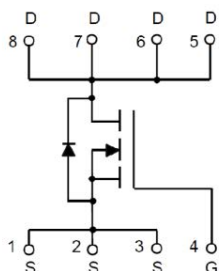


Top View



Bottom View

DFN3333-8L



Product Summary

- V_{DS} 100V
- I_D 50A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<12m\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) $<18m\Omega$
- 100% EAS Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ C$	I_D	8.6	A
	$T_A=100^\circ C$		6	
	$T_C=25^\circ C$		50	
	$T_C=100^\circ C$		35	
Pulsed Drain Current ^A		I_{DM}	200	A
Avalanche energy ^B		EAS	64	mJ
Total Power Dissipation ^C	$T_A=25^\circ C$	P_D	2.2	W
	$T_A=100^\circ C$		1.1	
	$T_C=25^\circ C$		78.5	
	$T_C=100^\circ C$		39	
Junction and Storage Temperature Range		T_J, T_{STG}	$-55 \sim +175$	$^\circ C$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	$R_{\theta JA}$	55	66	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.55	1.9	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCQ50G10A	F1	Q50G10A	5000	10000	100000	13" reel

SCQ50G10A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250uA	100	-	-	V
		V _{GS} = 0V, I _D =1mA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
		V _{DS} =100V, V _{GS} =0V, T _j =125°C	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1	1.7	3	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	9	12	mΩ
		V _{GS} =4.5V, I _D =20A	-	12	18	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V	-	-	1.2	V
Gate resistance	R _G	f=1MHz	-	1	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	50	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHz	-	1370	-	pF
Output Capacitance	C _{oss}		-	335	-	
Reverse Transfer Capacitance	C _{rss}		-	1.65	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =27.5A	-	27.9	-	nC
Gate-Source Charge	Q _{gs}		-	5	-	
Gate-Drain Charge	Q _{gd}		-	7.8	-	
Reverse Recovery Charge	Q _{rr}	I _F =27.5A, di/dt=100A/us	-	60	-	nC
Reverse Recovery Time	t _{rr}		-	44	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _D =27.5A R _{GEN} =2.2Ω	-	8.4	-	ns
Turn-on Rise Time	t _r		-	56	-	
Turn-off Delay Time	t _{D(off)}		-	24.4	-	
Turn-off fall Time	t _f		-	7	-	

- A. Repetitive rating; pulse width limited by max. junction temperature.
 B. T_J=25°C, V_G=10V, R_G=25Ω, L=0.5mH, I_{AS}=16A.
 C. P_g is based on max. junction temperature, using junction-case and junction-Ambient thermal resistance.
 D. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in the still air environment with T_A =25°C. The maximum allowed junction temperature of 175°C. The value in any given application depends on the user's specific board design.

■ Typical Electrical and Thermal Characteristics Diagrams

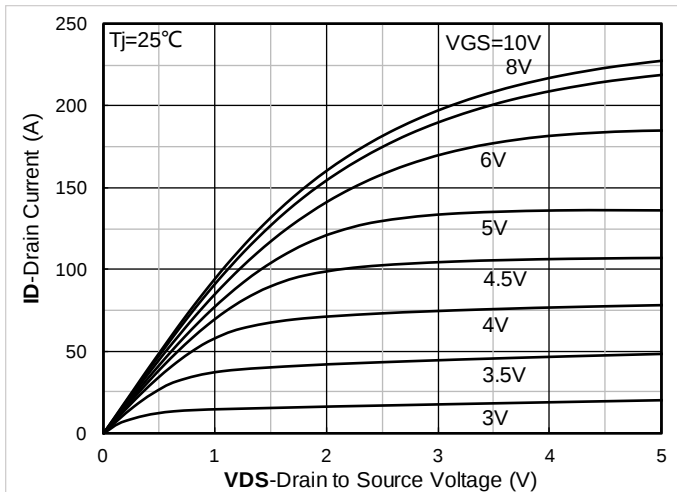


Figure 1. Output Characteristics

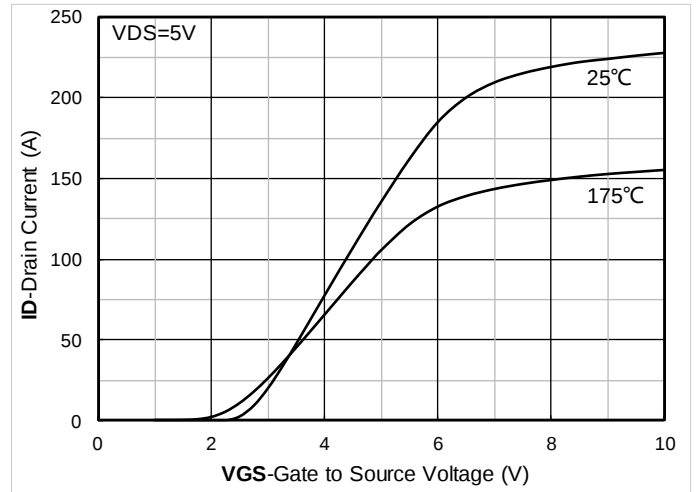


Figure 2. Transfer Characteristics

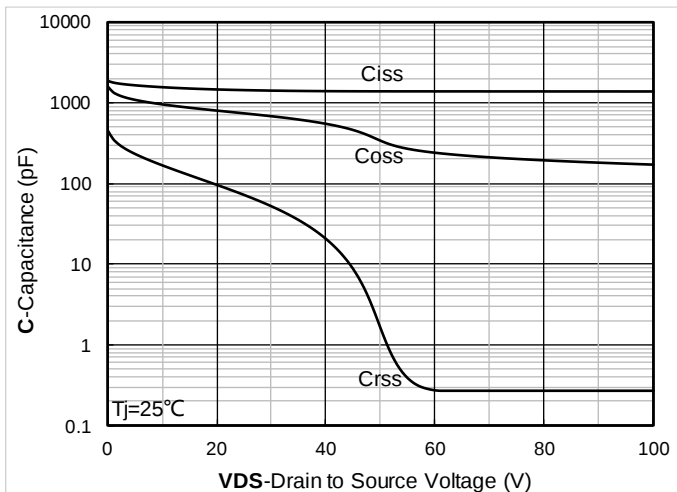


Figure 3. Capacitance Characteristics

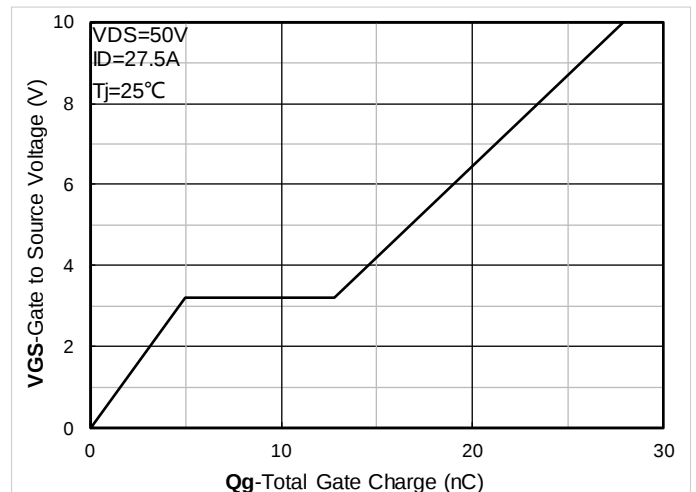


Figure 4. Gate Charge

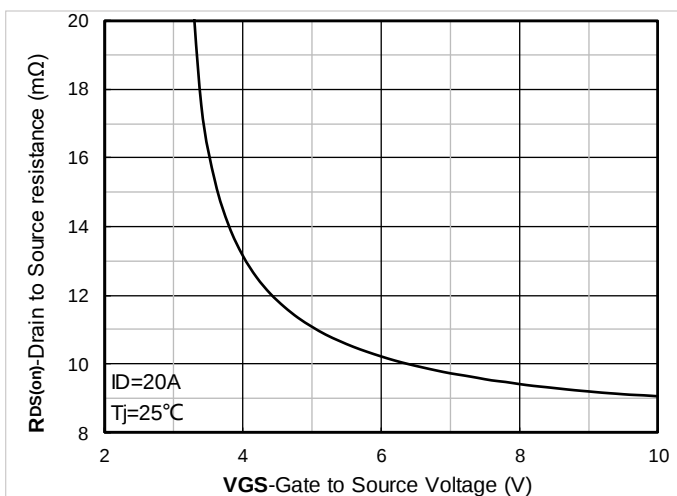


Figure 5. On-Resistance vs Gate to Source Voltage

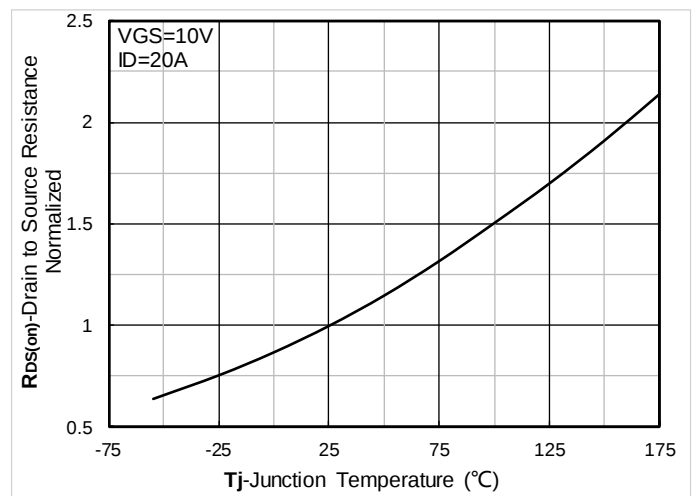


Figure 6. Normalized On-Resistance

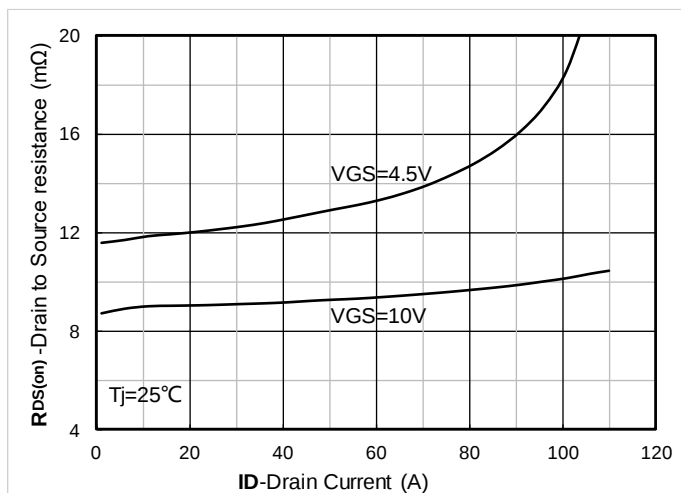


Figure 7. RDS(on) VS Drain Current

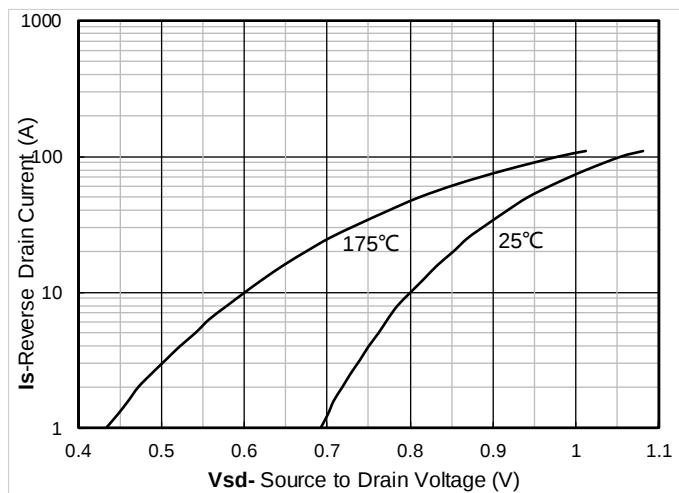


Figure 8. Forward characteristics of reverse diode

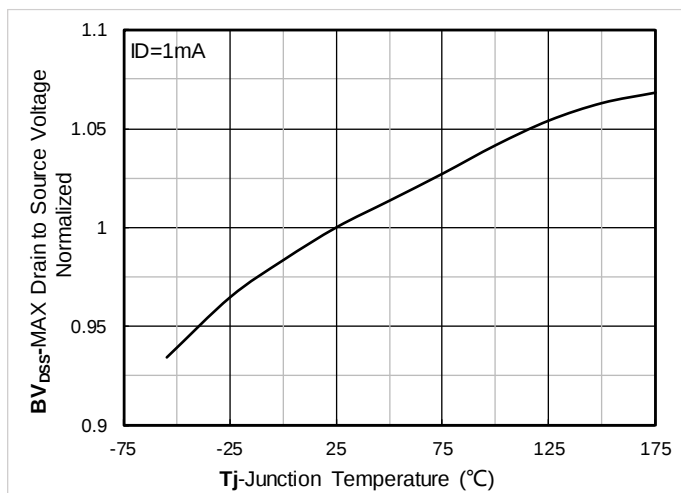


Figure 9. Normalized breakdown voltage

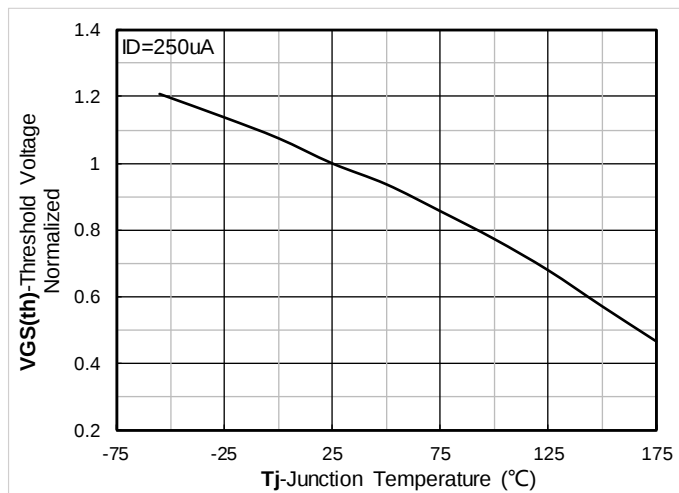


Figure 10. Normalized Threshold voltage

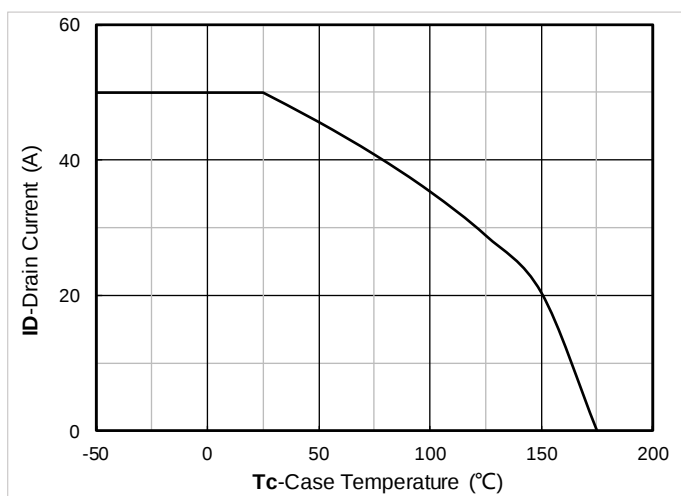


Figure 11. Current dissipation

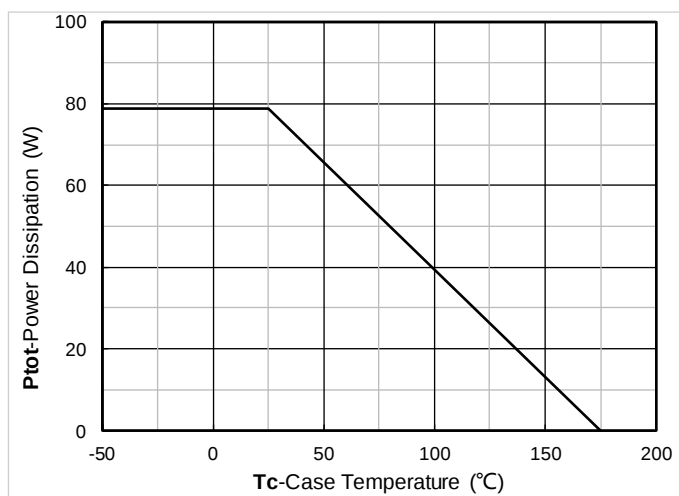


Figure 12. Power dissipation

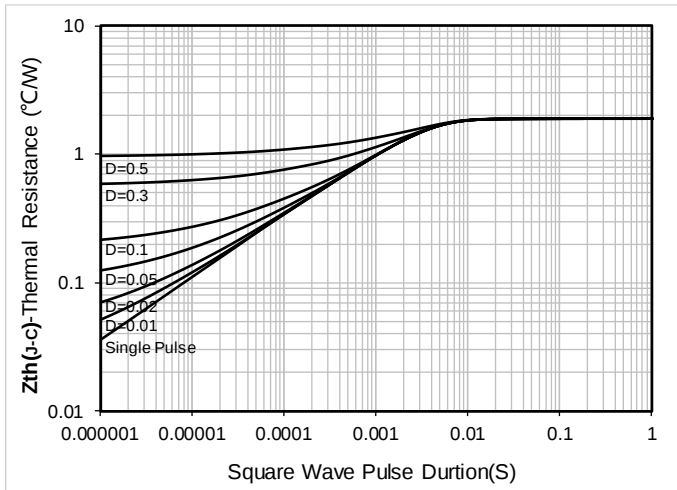


Figure 13. Maximum Transient Thermal Impedance

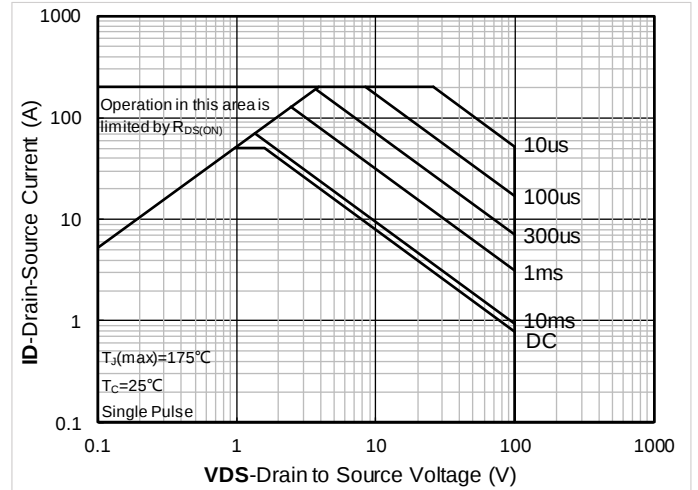


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

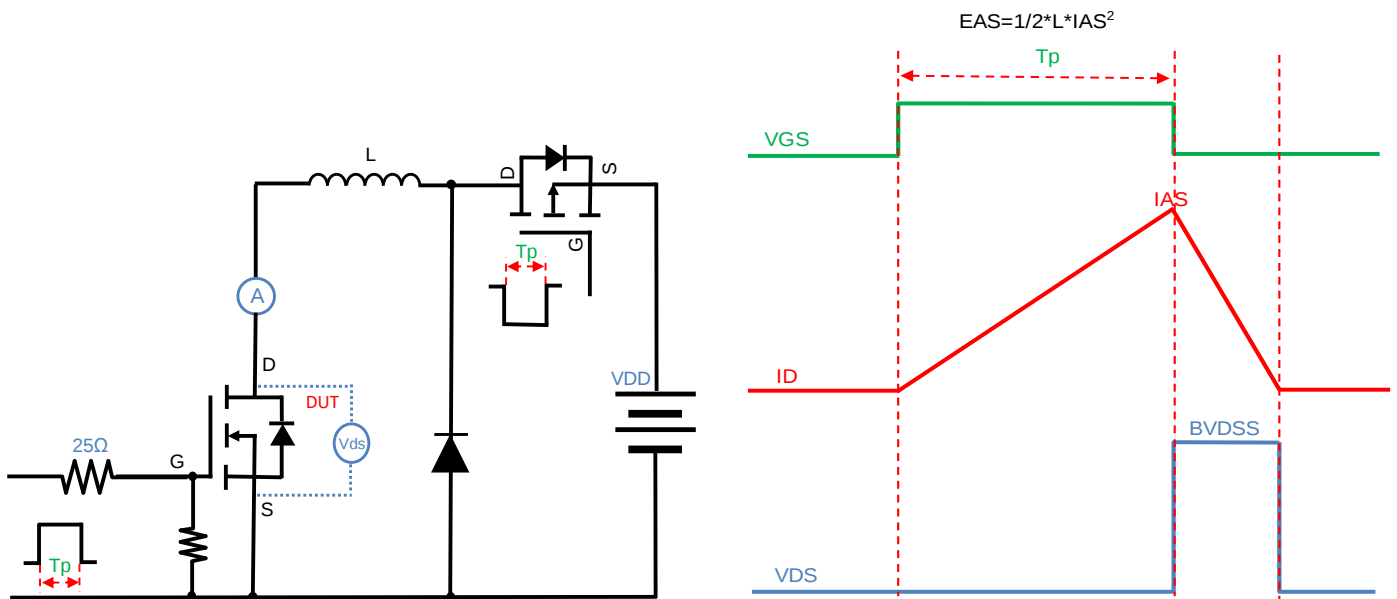


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform



Figure B. Gate Charge Test Circuit & Waveform

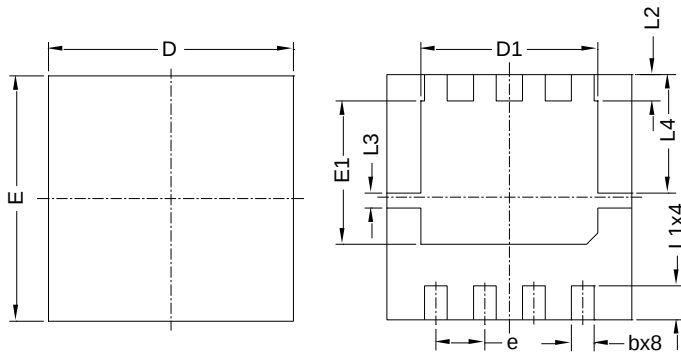


Figure C. Resistive Switching Test Circuit & Waveform



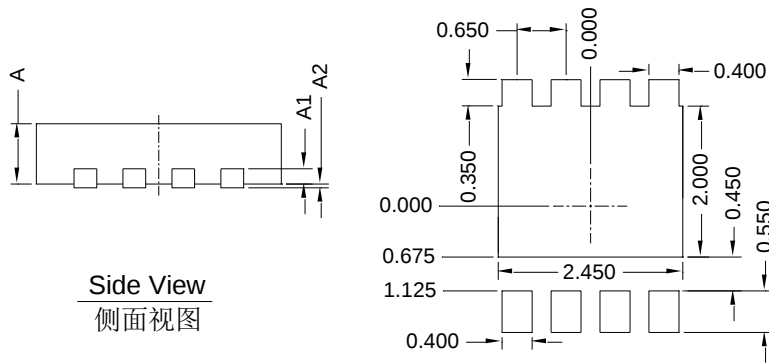
Figure D. Diode Recovery Test Circuit & Waveform

■ DFN3333-8L-A-0.8MM Package information



Top View
正面视图

Bottom View
背面视图



Side View
侧面视图

Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
L3	0.20 BSC		
L4	1.57 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.

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