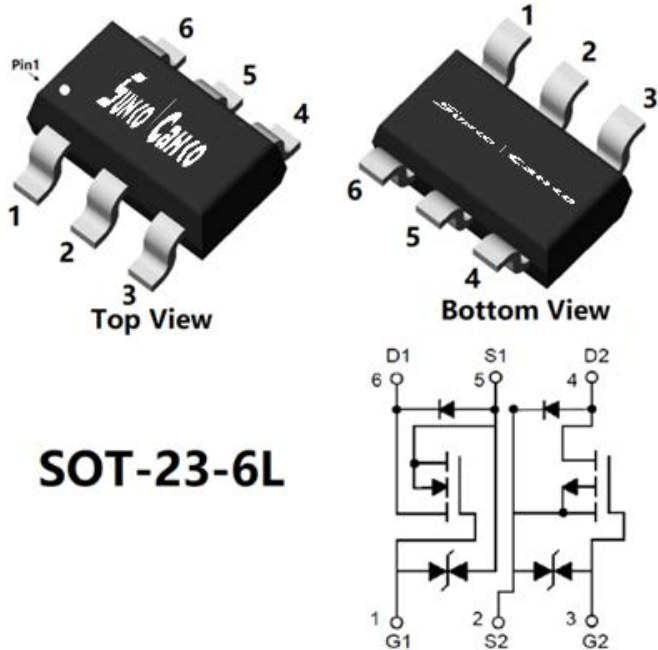


N-Channel and P-Channel Complementary Power MOSFET



Product Summary

NMOS(Die1)

- V_{DS} 20V
- I_D 0.5A
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <280 mohm
- $R_{DS(ON)}$ (at $V_{GS}=2.5V$) <400 mohm
- ESD Protected Up to 2.0KV (HBM)

PMOS(Die2)

- V_{DS} -20V
- I_D -0.5A
- $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) <850 mohm
- $R_{DS(ON)}$ (at $V_{GS}=-2.5V$) <1200 mohm
- ESD Protected Up to 2.0KV (HBM)

General Description

- Trench Power LV MOSFET technology
- High Density Cell Design for Low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Interfacing, Logic switch
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-source Voltage		V_{DS}	20	-20	V
Gate-source Voltage		V_{GS}	± 12	± 12	V
Drain Current	$T_C=25^\circ\text{C}$	I_D	0.5	-0.5	A
	$T_C=70^\circ\text{C}$		0.4	-0.4	
Pulsed Drain Current ^A		I_{DM}	2.3	-2.3	A
Total Power Dissipation	$T_C=25^\circ\text{C}$	P_D	0.3	0.3	W
Thermal Resistance Junction-to-Ambient @ Steady State ^B		$R_{\theta JA}$	416	416	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SCJ3439KA	F2	49KA	3000	30000	120000	7" reel

SCJ3439KA

■ N-MOS Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V,V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±10V, V _{DS} =0V		±1.5	±10	μA
		V _{GS} = ±8V, V _{DS} =0V		±500	±2000	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	0.35	0.75	1.1	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 4.5V, I _D =0.5A		180	280	mΩ
		V _{GS} = 2.5V, I _D =0.3A		250	400	
		V _{GS} = 1.8V, I _D =0.2A		420	650	
Diode Forward Voltage ^C	V _{SD}	I _S =0.5A,V _{GS} =0V			1.2	V
Maximum Body-Diode Continuous Current	I _S				0.5	A
Dynamic Parameters ^B						
Input Capacitance	C _{iss}	V _{DS} =10V,V _{GS} =0V,f=1MHZ		52		pF
Output Capacitance	C _{oss}			19		
Reverse Transfer Capacitance	C _{rss}			2.3		
Switching Parameters ^B						
Total Gate Charge	Q _g	V _{GS} =4.5V,V _{DS} =10V,I _D =0.5A		1		nC
Gate Source Charge	Q _{gs}			0.27		
Gate Drain Charge	Q _{gd}			0.21		
Reverse Recovery Charge	Q _{rr}	I _F =0.5A, di/dt=-20A/us		0.39		ns
Reverse Recovery Time	t _{rr}			14		
Turn-on Delay Time	t _{D(on)}	V _{GS} =4.5V,V _{DD} =10V,R _G =10Ω,I _D =500mA		2.1		
Turn-on Rise Time	t _r			17.5		
Turn-off Delay Time	t _{D(off)}			9.5		
Turn-off Fall Time	t _f			22		

A. Pulse Test: Pulse Width≤300us, Duty cycle ≤2%.

B. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch.

SCJ3439KA

■ P-MOS Electrical Characteristics (TJ=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V,V _{GS} =0V,T _C =25℃			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±10V, V _{DS} =0V		±1.5	±10	μA
		V _{GS} = ±8V, V _{DS} =0V		±500	±2000	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-0.35	-0.62	-1.2	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = -4.5V, I _D =-0.5A		610	850	mΩ
		V _{GS} = -2.5V, I _D =-0.3A		930	1200	
		V _{GS} = -1.8V, I _D =-0.2A		1100	1700	
Diode Forward Voltage	V _{SD}	I _S =-0.5A,V _{GS} =0V			-1.2	V
Maximum Body-Diode Continuous Current	I _S				-0.5	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-10V,V _{GS} =0V,f=1MHZ		70		pF
Output Capacitance	C _{oss}			19		
Reverse Transfer Capacitance	C _{rss}			14		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-4.5V,V _{DD} =-10V,I _D =-0.5A		1.22		nC
Gate Source Charge	Q _{gs}			0.36		
Gate Drain Charge	Q _{gd}			0.26		
Reverse Recovery Chrage	Q _{rr}	I _F =-0.5A, di/dt=-20A/us		0.95		ns
Reverse Recovery Time	t _{rr}			24		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-4.5V,V _{DD} =-10V, R _L =2.5Ω, R _{GEN} =3Ω		4.5		
Turn-on Rise Time	t _r			18		
Turn-off Delay Time	t _{D(off)}			15		
Turn-off Fall Time	t _f			23		

- A. Pulse Test: Pulse Width $\leq 300\mu s$, Duty cycle $\leq 2\%$.
B. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch.

■ N-MOS Typical Performance Characteristics

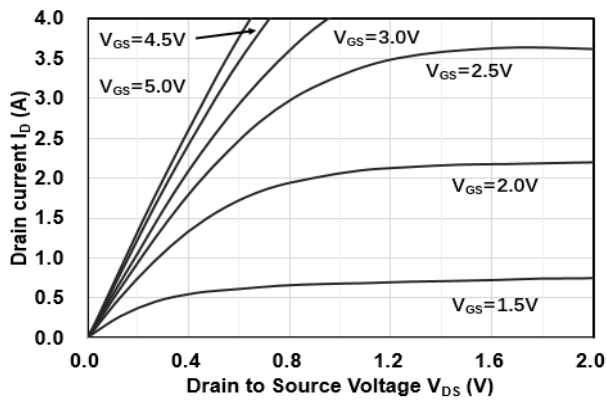


Figure1. Output Characteristics

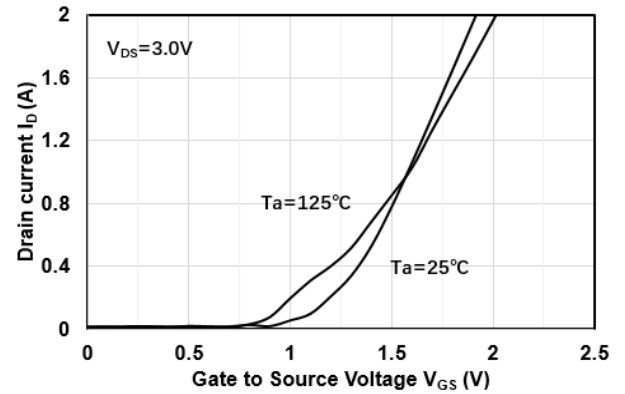


Figure2. Transfer Characteristics

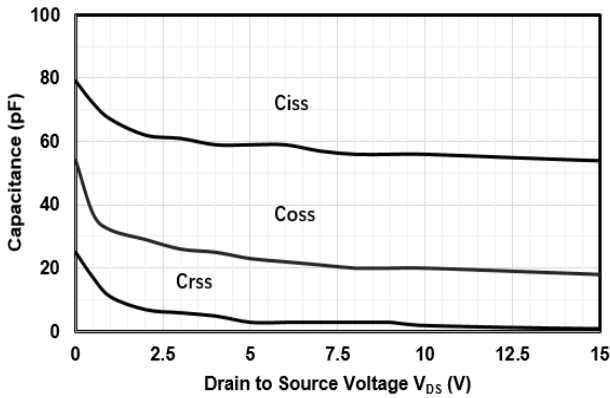


Figure3. Capacitance Characteristics

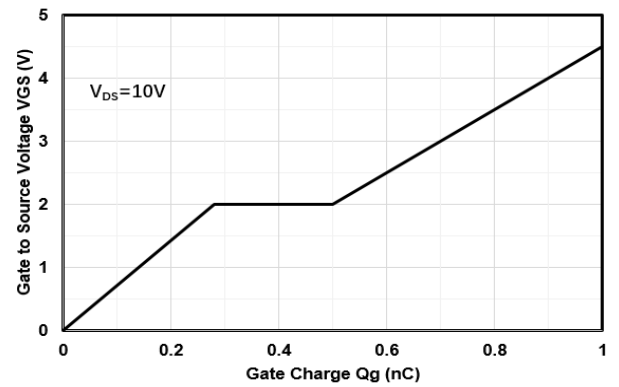


Figure4. Gate Charge

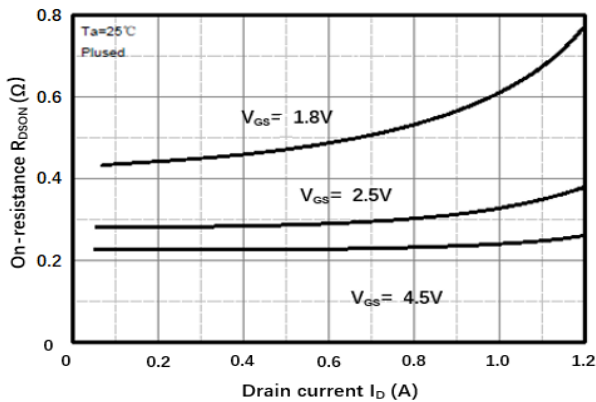


Figure5. Drain-Source on Resistance

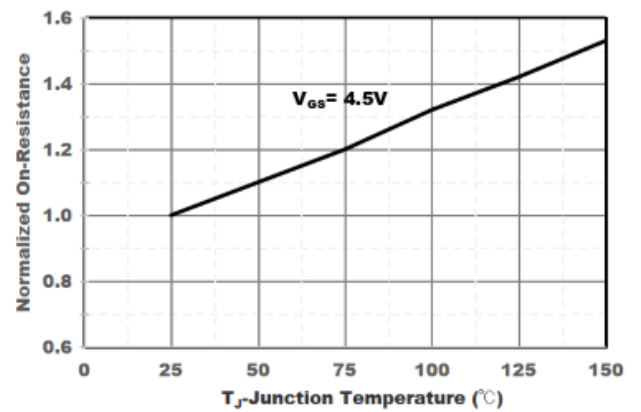


Figure6. Drain-Source on Resistance

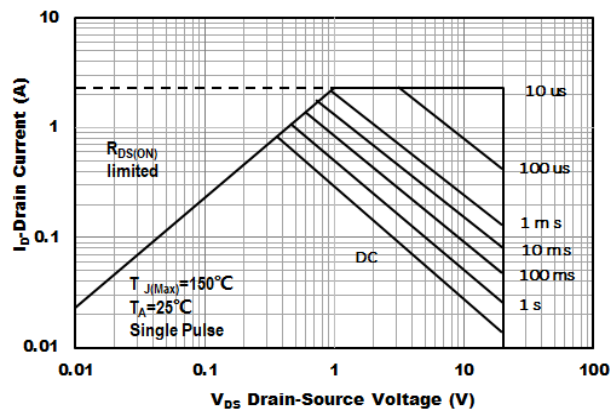


Figure7. Safe Operation Area

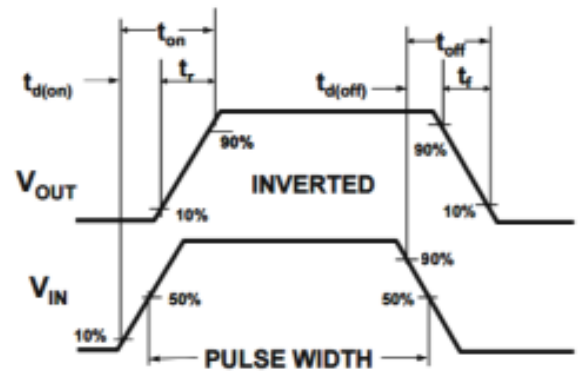


Figure8. Switching wave

■ P-MOS Typical Performance Characteristics

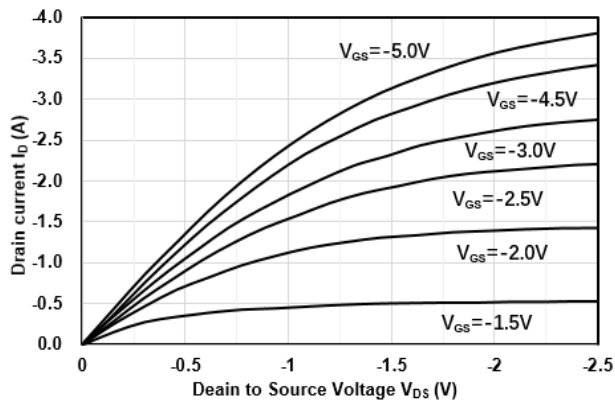


Figure1. Output Characteristics

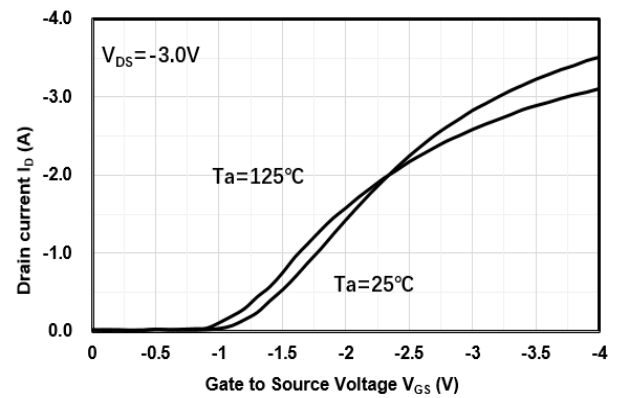


Figure2. Transfer Characteristics

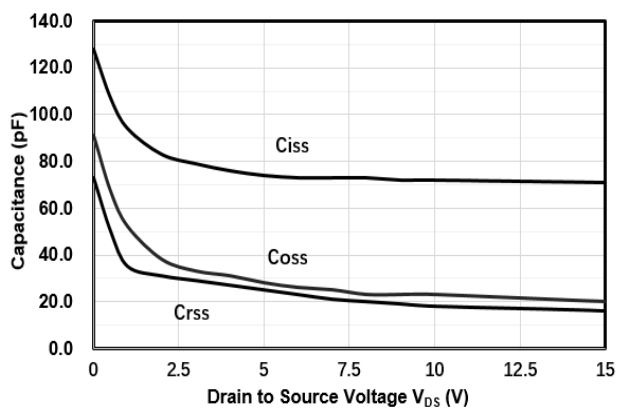


Figure3. Capacitance Characteristics

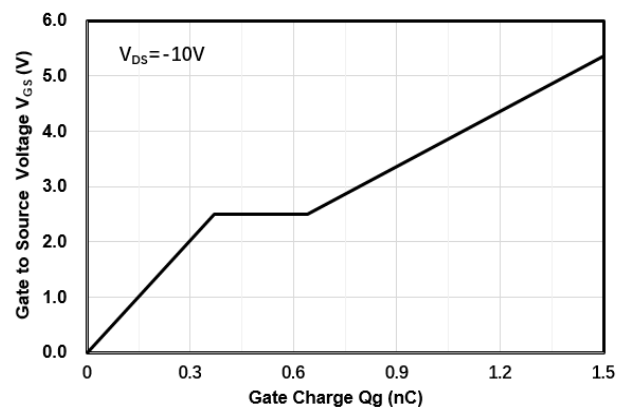


Figure4. Gate Charge

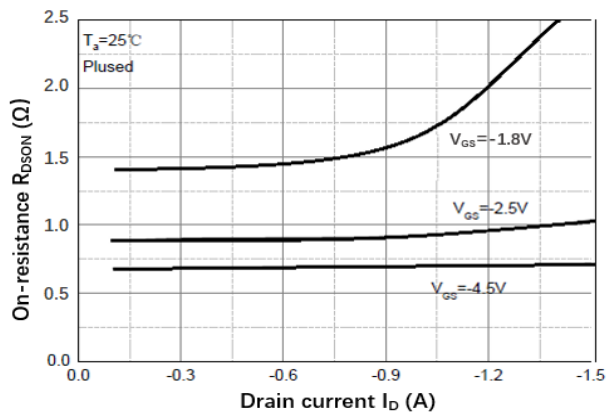


Figure5. Drain-Source on Resistance

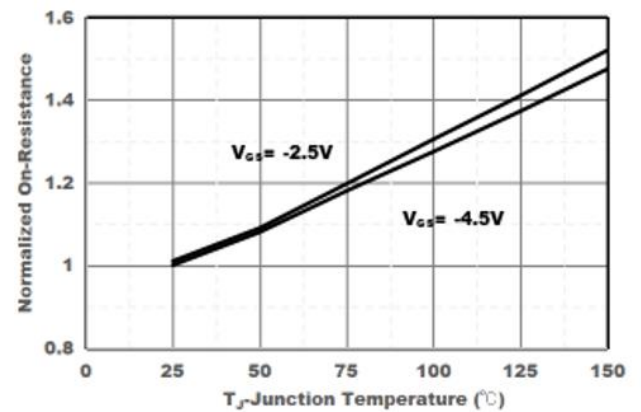


Figure6. Drain-Source on Resistance

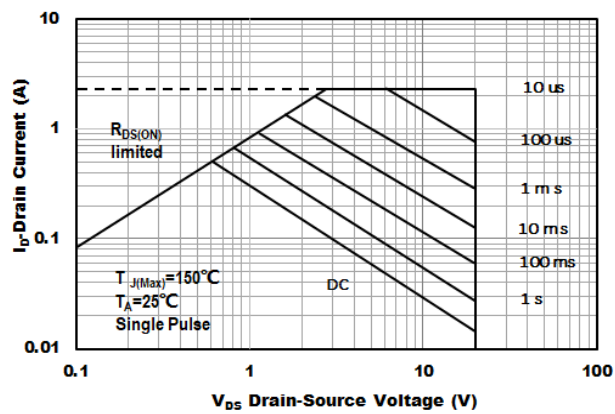


Figure7. Safe Operation Area

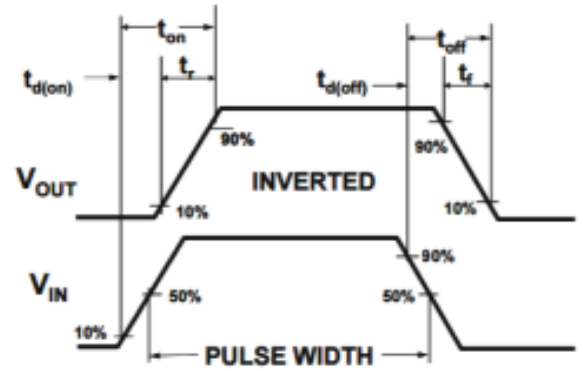
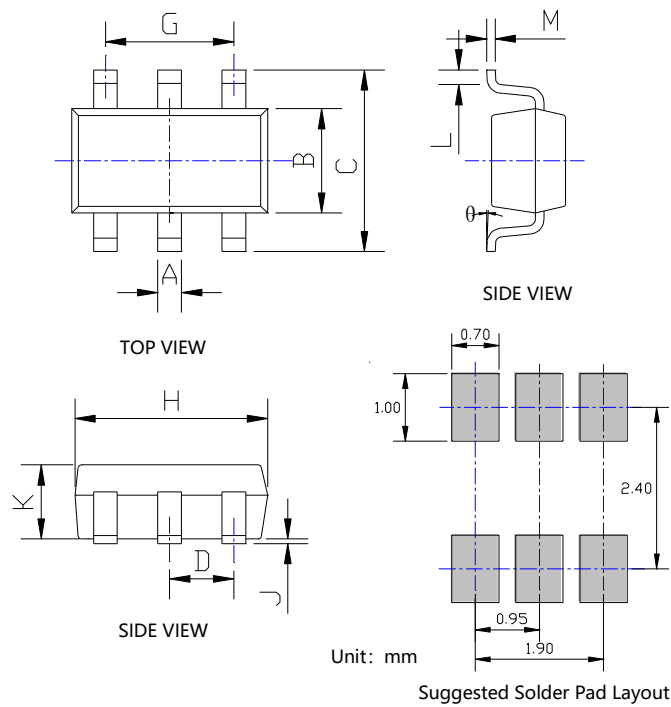


Figure8. Switching wave

■ SOT-23-6L Package Information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.012	0.020	0.300	0.500
B	0.059	0.067	1.500	1.700
C	0.104	0.116	2.650	2.950
D	0.037BSC		0.950BSC	
G	0.075BSC		1.900BSC	
H	0.111	0.119	2.820	3.020
J	0.000	0.004	0.000	0.100
K	0.041	0.045	1.050	1.150
L	0.012	0.024	0.300	0.600
M	0.004	0.008	0.100	0.200
θ	0°	8°	0°	8°

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.

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